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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,972	11/11/2003	Jing-Horng Gau	NAUP0538USA	2971
27765	7590	02/18/2005	EXAMINER	
NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC) P.O. BOX 506 MERRIFIELD, VA 22116			LUK, OLIVIA T	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/605,972	<b>Applicant(s)</b> GAU, JING-HORNG	
	<b>Examiner</b> Olivia T. Luk	<b>Art Unit</b> 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Stolfa et al. (5,965,912).

In re claim 1, Stolfa et al. disclose providing a substrate **12**, the substrate comprising an ion well of a first conductivity type **15** and a plurality of isolation structures **18** positioned on the ion well, the isolation structures defining at least an active area on the ion well; implanting ions of the first conductivity type into the ion well to form a doping region within the active area (col. 2, lines 38-50); forming a doping layer of a second conductivity type **22, 24, 26, 28** on the substrate **12** to cover portions of the doping region, and forming a salicide layer **81-89** (col. 4, lines 59-64) on the doping region and the doping layer.

In re claims 2 and 11, Stolfa et al. disclose forming a salicide block on the doping layer to prevent a junction between the doping region and the doping layer from being destroyed by the salicide layer (col. 4, lines 58-64).

In re claims 3 and 12, Stolfa et al. disclose at least a buried doping region **15** of the first conductivity type positioned beneath the ion well (col. 2, lines 34-36).

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In re claim 4, Stolfa et al. disclose at least a CMOS transistor (col. 1, lines 62-65), and the doping region of the varactor and a lightly doped drain of the CMOS transistor are formed using the same doping process (bridging paragraph between col. 2, and col. 3).

In re claim 5, Stolfa et al. disclose before forming the doping layer, the method further comprises forming at least a protective CMOS transistor (see bridging paragraph between col. 2, and col. 3).

In re claims 6 and 13, Stolfa et al. disclose the doping layer comprises an epitaxial layer 16 (col. 2, lines 63-65).

In re claims 7 and 14, Stolfa et al. disclose the doping layer comprises a polysilicon layer (col. 8, lines 15-24).

In re claims 8 and 15, Stolfa et al. disclose an ion implantation process to implant ions of the second conductivity type into the doping layer to adjust the resistance of the doping layer (col. 2, lines 51-67).

In re claims 9 and 16, Stolfa et al. disclose a doping concentration of the doping region is higher than a doping concentration of the ion well (col. 2, lines 51-67).

In re claim 10, Stolfa et al. disclose implanting ions of a first conductivity type 15 into the substrate 12 to form at least a first ion well 15 in the first region and at least a second ion well 18 in the second region, implanting ions of a second conductivity type into the substrate to form at least a third ion well 22, 24, 26, 28 in the first region forming a plurality of isolation structures on the substrate (col. 2, lines 11-67); forming a first gate 62, 64 on the first ion well and a second gate 66, 68 on the third ion well, implanting ions of the first conductivity type into the substrate to form two first lightly doped drains on the third ion well (col. 2, lines 35-65), and

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simultaneously form a doping region on the second ion well; implanting ions of the second conductivity type into the substrate to form two second lightly doped drains on the first ion well; forming a spacer **63, 65, 67, 69** on both sides of the first gate and on both sides of the second gate; forming two first source/drain regions of the second conductivity type on the first ion well (see Fig. 2), and forming two second source/drain regions of the first conductivity type on the third ion well (see Fig. 2); forming a protective layer **16** on the substrate **12**, the protective layer comprising an opening to expose the doping region (col. 2, lines 60-62); forming a doping layer of the second conductivity type on doping region (col. 2, lines 64-66), and performing a salicidation process to on the substrate to form a salicide layer **82, 84, 86, 88** (col. 4, lines 35-67).

### *Conclusion*

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References not applied are considered state of the art in the area of semiconductor manufacture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Olivia T. Luk whose telephone number is 571-272-1676. The examiner can normally be reached on 8AM to 5PM Mon-Fri.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

OTL

February 11, 2005

  
MICHAEL S. LEBENTRITT  
PRIMARY EXAMINER